Kirkendall voiding in Au ball bond interconnects on Al chip metallization in the temperature range from 100 – 200°C after optimized intermetallic coverage

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Abstract

The presentation addresses the reliability of Au ball bonds of different Au wire qualities on Al chip metallizations of different thicknesses and compositions at temperature storage from 100 to 200°C up to 4000 h. In this context the interfacial reactions and intermetallic phase coverage directly after the bonding process was optimized to get the best starting condition for phase growth at elevated temperatures and to avoid critical Kirkendall void growth.

This failure mechanism is influenced by numerous factors, such as aging temperature and time, Au wire and Al metallization composition and ratio of mixture as well as the percental area of interconnection formation under the ball. These influences are mainly responsible for ball lift offs under operating conditions. In many cases lift offs already occur at Al metallization thicknesses > 1 µm and temperatures in the range of 175°C, while temperatures up to 150°C or at 200°C are less critical.

Investigations include mechanical tests of Au loops and ball contacts as well as microstructure observations of the contacts in correlation to material composition, aging temperature and Al metallization thickness. Au/Al intermetallic phase thicknesses below the Au contacts on Al metallization are typically a few hundred nanometers thick directly after the bonding process, depending on bonding conditions like process parameters and material combination. These phases grow under temperature influence and Kirkendall voiding can occur. A most significant result in this context is that pull and shear lift offs occur if the chip metallization is clearly thicker than 1 µm and intermetallic phase coverage (after bonding) is less than 2/3 of the bottom side ball area.

These results will considerably contribute to a better understanding of Kirkendall voiding failure mechanisms.

Key words: Au wire bonding, Al chip metallization thickness, interface formation, Au-Al intermetallic phases

Introduction

Wire bonding continues to be popular and dominant in the field of bonding technologies in the industry. Thermosonic bonding is used for Au and Cu wires and currently comprises about 90% of all wire bonding interconnections. Interdiffusion, intermetallic phase (IP) growth and Kirkendall voiding in Au ball bond on Al chipmetallization systems at temperature storage is in discussion since ball/wedge wire bonding in microelectronic packing was developed. Today this is of very special interest in various microelectronic application fields (e.g. automotive) because more and more maximum operating temperatures exceed 150°C.

The failure mechanism Kirkendall voiding often results in ball lifting from chip metallization. The most influential factors are the bonding parameters [1-3] including tool geometry (capillary) [4-5] and the transducer frequency [6]. The ball bond intermetallic coverage is one of the most important boundary conditions for interconnection reliability at high temperature storage (≥ 150°C) where massive IP growing occurs [2, 3]. In addition to temperature and storage duration, thickness and chemical composition of Al metallizations have to be considered. Alloying state of Au wires and contaminations are other typical influencing factors relating to growth of IPs and - more critical - Kirkendall voids [7-9].

The paper presents results of tempering Au ball bonds of different Au ball qualities on various Al chip metallizations after optimizing the interconnection formation and IP coverage. Main finding is that Au ball lift offs from Al metallizations can be eliminated even in the critical temperature range of 170 – 180°C if metallization is AlSiCu and the thickness is smaller then 1 µm. Another important result is the recommendation to optimize the IP coverage up to 90% and don´t use pure Al metallizations if possible.

Bonding of different Au wires on different chips

TS Au wire bonding (25 µm) was carried out on a standard bonding machine (ESEC 3088 Ball/Wedge-Bonder) with a transducer frequency of 120 kHz at 125°C work holder temperature and capillary UTS-38-C-1/16-XL (SPT). Chips with 4 different Al metallizations were glued on ceramic substrates with Au thick film metallizations and interconnected with 4 different Au wires (Table 1).

Table 1: Materials and properties

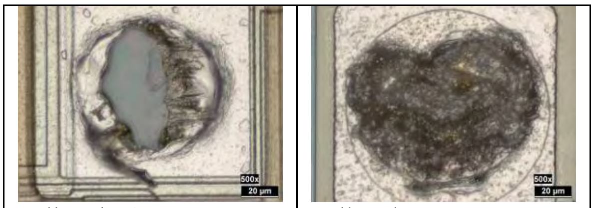
material	notation	parameter
Au bond wire 25 µm	K&S Radix Plus (3N pure)	break. load 10.8 cN elongation 4.6%
	K&S AW99 (4N pure, Be free)	break. load 12.6 cN elongation 4.0%
	Heraeus HA3 (2N plus 1% Pd)	break. load 13.3 cN elongation 4.3%
	Heraeus HA9 (4N pure)	break. load 11.8 cN elongation 4.6%
chip metal-lization	chip A	2 µm Al
	chip B	4 µm AlSiCu
	chip C	4.4 µm AlSiCu
	chip D	0.8 µm AlSiCu

The evaluation of bonding series was performed by shear testing (ball bond) on XYZTec test equipment and KOH etching (10 min) of Al metallization to determinate the IP coverage beneath the balls. Pull testing was done on Dage 4000 test equipment.

The failure codes of pull and shear test before and after temperature storage up to 200°C are summarized in Table 2 and Table 3. Views of characteristic pull and shear codes are shown in Figure 1 and Figure 2. The initial pull and shear test results after parameter optimization are summarized in Table 4 (20 tests each combination).

Table 2: Pull test codes

pull code	failure mode
2	neck crack (over ball)
6	ball lift off including metallization / IP
7	ball lift off (interface IP)



pull code 6 | pull code 7

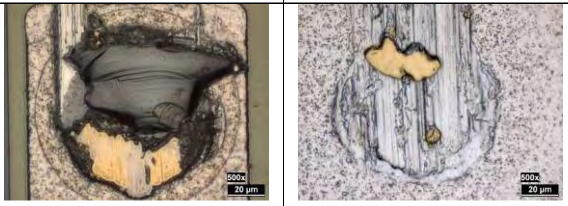
Figure 1: Typical appearance of critical pull codes

Table 3: Shear test codes

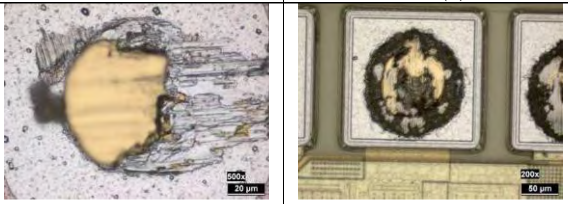
shear code	failure mode
3	ball shear (shearing through the ball)
4	metallization lift off
5	cratering
6	mixed mode* at high shear forces
7	mixed mode* at lower shear forces

* Partial crack in chip metallization, in the ball and at the interface

shear code 3 | shear code 4



shear code 5 | shear code 6 (a)



shear code 6 (b) | shear code 7

Figure 2: Typical appearance of shear codes

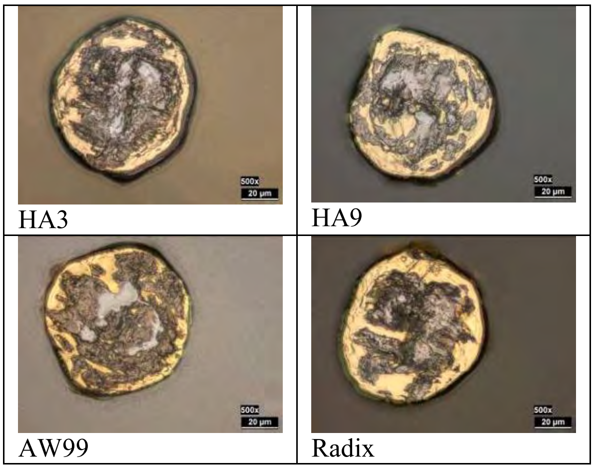
After bonding parameter optimization the initial state of bonding quality was characterized by the absence of pull or shear lift offs which indicates a good interconnection. These good initial bonding results were confirmed by a high degree of IP formation at the interface Au ball / Al chip metallization as to be seen at the bottom side of the Au balls after KOH etching (see **Figure 3**, chip D). For all 12 chip / wire combinations the IP coverage directly after the bonding process was proofed to be greater than 2/3 of the bottom side ball area.

At last cross sections were made to investigate the IP growth and void formation after temperature storage and to compare it with the mechanical test results.

Table 4: Initial pull and shear test results (n = 20)

wire/chip combination	pull test *		shear test			
	X	σ	X	σ	s3	s6
HA3 chip A	12.7	0.4	62.5	5.8	0	20
HA3 chip B	13.5	0.4	56.4	4.9	0	20
HA3 chip C	12.8	0.4	51.9	3.5	0	20
HA3 chip D	13.4	0.7	62.2	2.8	0	20
HA9 chip A	11.2	0.3	76.7	2.9	0	20
HA9 chip B	11.6	0.4	57.3	4.9	15	5
HA9 chip C	11.1	0.3	62.4	4.5	14	6
HA9 chip D	11.8	0.3	65.5	8.7	6	14
AW99 chip A	10.8	0.2	58.1	3.2	2	18
AW99 chip B	11.4	0.3	58.2	7.5	6	14
AW99 chip C	10.9	0.3	52.4	4.4	0	20
AW99 chip D	11.6	0.3	58.2	6.1	0	20
Radix chip A	11.2	0.3	48.9	3.0	0	20
Radix chip B	12.0	0.4	51.1	4.5	0	20
Radix chip C	11.1	0.6	56.4	5.5	0	20
Radix chip D	11.9	0.3	52.4	4.3	0	20

* only neck breaks; X: Mean value in cN; σ: standard deviation in cN; s3/s6: number of shear code 3 resp. 6



HA3

HA9

AW99

Radix

Figure 3: IP coverage underneath the balls directly after bonding and KOH etching (chip D)

Temperature storage test results and discussion

All bonding samples for reliability investigations were bonded with optimized bonding parameters and annealed in laboratory furnaces. Test temperatures and time intervals for mechanical testing were ascertained as follows:

- 100°C – 150°C: 24, 96, 250, 500, 1000, 1500, 2000 and 4000 h (140°C up to 5000 h)
- 160°C – 200°C: 4, 8, 24, 48, 96, 250, 500, 1000, 2000 and 4000 h

Best results could be achieved with the combination of chip D with the thin AlSiCu metallization and the 3N pure Radix Plus Au wire as to be seen in Figure 4 and Figure 5 where at all temperatures and test intervalls pull and shear forces were more or less at the same level and no pull and shear lift offs occurred. At all other 2.0 – 4.4 µm thick Al metallizations pull lift offs appeared. Worst case occurred with the thickest AlSiCu metallization (4.4 µm) of chip C with poorest pull test results in combination with the 4N pure AW99 Au wire (Figure 6 and Figure 7) and poorest shear test results in combination with the 2N pure HA3 Au wire (Figure 8 and Figure 9).

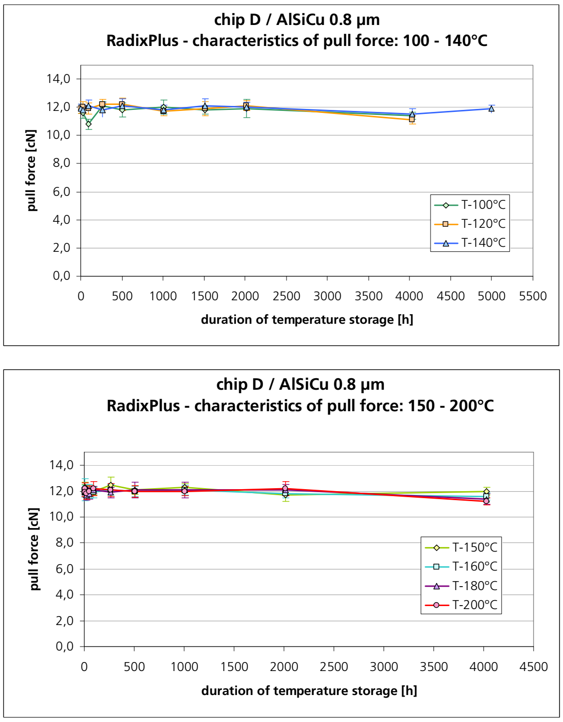


Figure 4: Pull test results Radix / chip D

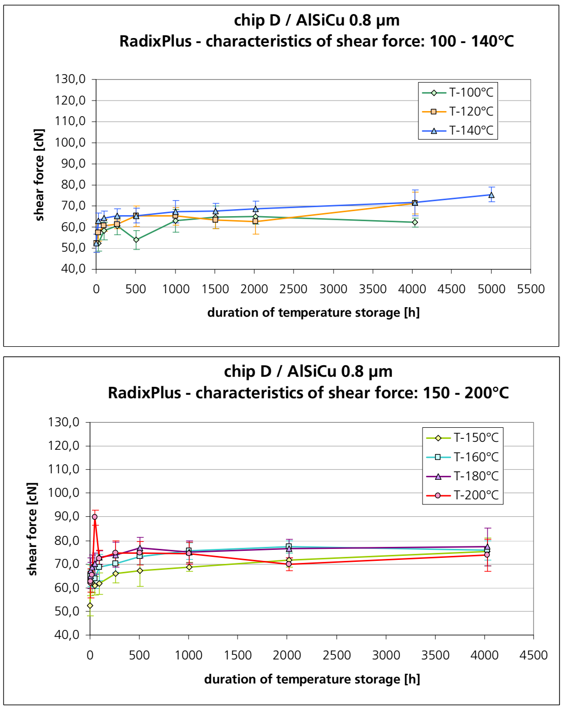


Figure 5: Shear test results Radix / chip D

Pull lift offs with pull force values below 4 cN are very critical. This was especially the case at 200°C above 1000 h storage duration where 7 of 11 pull lift offs occurred with pull force values between 2.1 and 3.7 cN (s. the red bars and high standard deviations in Figure 7).

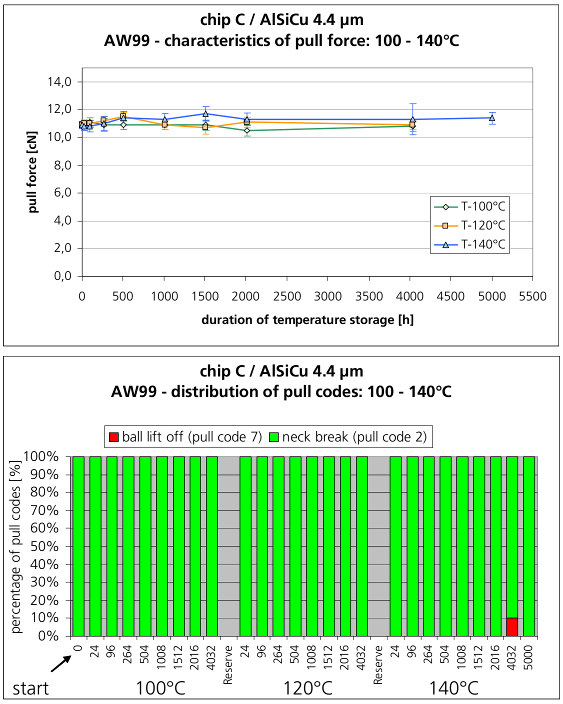


Figure 6: Pull test results AW99 / chip C (100 - 140°C)

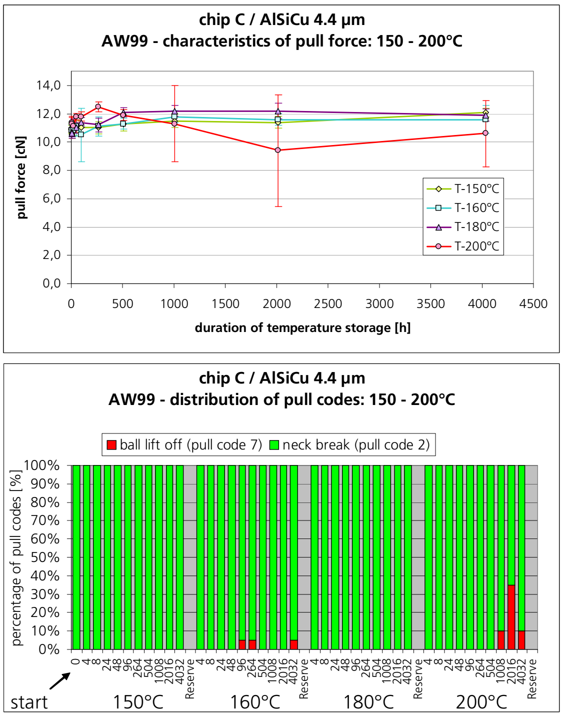


Figure 7: Pull test results AW99 / chip C (150 - 200°C)

The red bars in Figure 8 and Figure 9 indicate the shear code 7 with a fracture running partially in the chip metallization, in the ball and at the interface (Figure 2) at shear force values less than 60 cN. In these cases starting interface degradations caused by Kirkendall voiding can be assumed.

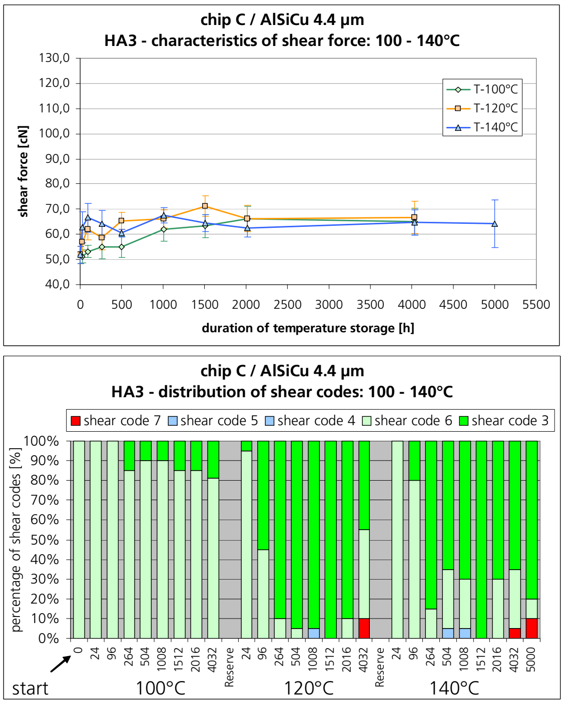


Figure 8: Shear test results HA3 / chip C (100 - 140°C)

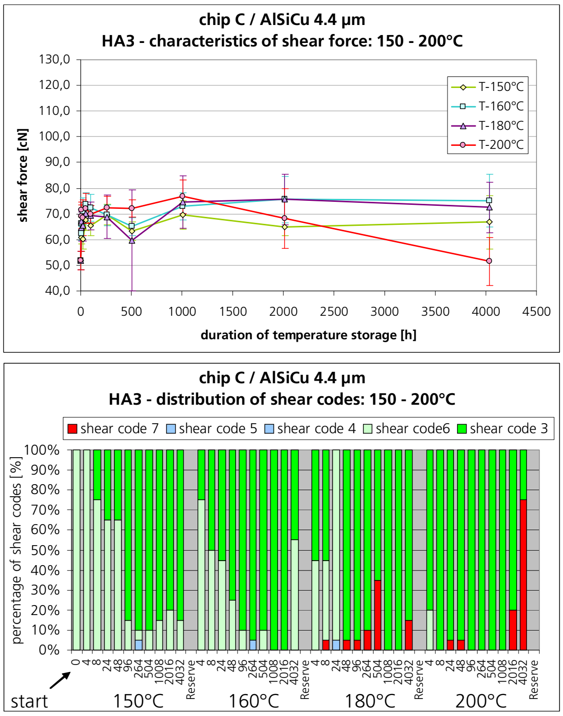


Figure 9: Shear test results HA3 / chip C (150 - 200°C)

Cross sections of Au HA3 ball bonds on chip C after 4000 h of temperature storage at 200°C give an example for Kirkendall voiding in Figure 10. Different intermetallic phases are visible between ball and chip. Despite the very long duration at high storage temperature the interdiffusion processes were not finished. This is caused by the chip pad size (165 µm x 165 µm) and Al thickness of 4.4 µm and therefore availability of Al for interdiffusion and phase formation as well as the lower diffusion coefficients of Au wires which are alloyed with Pd. But none of all measured shear force values of this shear code 7 (on all chips) was smaller than 25 cN. If these pore constellations underneath the balls are critical under application and realibility aspects needs to be discussed.

More critical to evaluate are pull lift offs with single pull force value below 4 cN for all investigated Au wires with initial breaking loads above 10 cN. Therefore all quantified pull lift offs are summarized in Table 5. Values are red-marked if pull force undercut 4 cN.

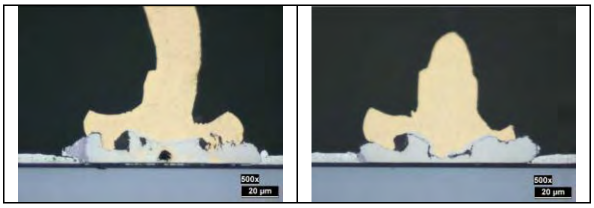
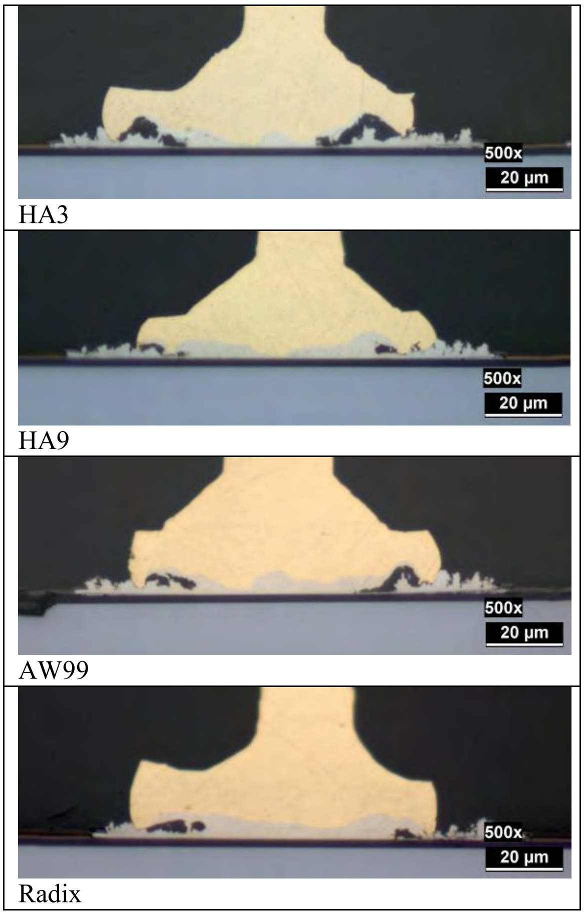


Figure 10: Cross sections of HA3 Au balls on chip C after 4000 h at 200°C

Table 5: Compilation of all pull lift offs

chip	wire	t [h]	T [°C]	pull force [cN]
A	HA9	250	200	4.5
B	HA3	1000	140	11.9
B	HA3	1000	180	7.0
B	HA3	24	150	7.1
B	HA3	96	150	8.6
B	HA3	500	150	10.9
B	HA3	2000	150	12.4
B	HA9	500	200	10.3
B	Radix	4000	150	7.2 and 12.1
C	HA3	500	200	3.0
C	HA3	500	200	7.0
C	HA3	2000	200	9.4
C	HA9	4000	200	7.7 and 8.0
C	AW99	4000	140	7.5 and 9.0
C	AW99	96	160	2.5
C	AW99	250	160	9.0
C	AW99	4000	160	7.8
C	AW99	1000	200	3.0 and 3.7
C	AW99	2000	200	2.1 and 3.2
C	AW99	2000	200	3.2 and 3.3
C	AW99	2000	200	4.5 and 7.2
C	AW99	2000	200	8.0
C	AW99	4000	200	3.0
C	AW99	4000	200	5.0

As to be seen very clearly in Table 5 critical Au ball pull lift offs occurred only on the thickest Al pad metallization of chip C with the biggest pad dimension of approx. 165 µm x 165 µm additionally. The pad sizes of the other chips A, B and D were smaller with edge lengths in the range of 100 µm – 120 µm. Some other pull lift offs at pull force values above 4 cN appeared on chip B with Al thickness of 4 µm and one on chip A with 2 µm Al. On chip D with only 0.8 µm Al thickness no lift offs occurred. After longer storage duration at higher temperature all Al of the chip metallization was transformed to intermetallic phases respectively in Au_4Al after 4000 h at 200°C (Figure 11).



HA3

HA9

AW99

Radix

Figure 11: Intermetallic phase formation on chip D after 4000 h at 200°C

The strength of the ball bond interconnections was high enough despite a lot of gaps at the interface (s. Figure 11) as a result of Kirkendall voiding as well as volume expansion through interdiffusion resulting in intermetallic phase formation and growth. This is a result of higher strength of intermetallic Au/Al phases compared to metallic Au or Al. No pull lift offs appeared on chip D with all wire types and all pull force values were above 10 cN in all cases.

Compared to the results in [9] where a hard degradation with lift offs at very low pull force values was determined there is only a marginal count of Au ball lift offs in the investigation presented in this paper on chips with thicker Al tempered in the critical temperature range from 160 – 180°C. Presumed reason for this divergence is that in [9] the IP coverage underneath the balls wasn´t optimized and controlled with KOH etching. Ball bond optimization in [9] was checked through mechanical tests only.

The conclusion can be drawn that there must be a direct correlation between the reliability of Au ball bonds on Al chip metallization at temperature storage and the Al thickness on the one hand and the intermetallic coverage directly after bonding on the other.

Conclusions

Reliability test results of different Au wires which were ball/wedge bonded with optimized parameters on different Al metallizations and tempered in the range from 100 - 200°C have been presented in this paper. The initial IP coverage underneath the balls was inspected after KOH etching and found to be in the range from 75 - 90% of the bottom side ball area. The interface strengths were tested before and after temperature storage by pull and shear tests and correlated to intermetallic phase growing and Kirkendall voiding by microstructural investigations on cross sections.

Main result is a correlation between the thickness and the alloying state of Al chip metallization and the appearance of ball lift offs. The failure mechanism is Kirkendall voiding during intermetallic phase formation and growth until gap formation underneath the ball is complete and ball lift off occurs. This failure mechanism is influenced by numerous factors, such as aging temperature and time, Au wire type and Al metallization composition and thickness as well as the percental area of interconnection formation (IP coverage) under the ball directly after bonding. Most lift offs occur with pure Al metallizations and thicknesses >> 1 µm. But it can be confirmed that it is possible to temper Au ball bonds on Al Chip metallization up to 200°C up to 4000 h without the occurrence of lift offs at mechanical tests if AlSiCu chip metallizations with thicknesses smaller than 1 µm are used and the IP coverage directly after the bonding process is nearly 90% of the bottom side ball area, even at the well known very critical storage temperature in the range of 175°C.

For practical work it can be recommended to use alloyed Al finish metallizations on chips (e.g. AlSi1Cu0.5) with reduced Al thickness (max. 1 µm) and to optimize the initial IP coverage to minimize the risk of ball lifting while tempering at elevated temperatures.

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